NEC

MOS INTEGRATED CIRCUIT
μPD75P238

4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P238 is a version of the μPD75238 in which the on-chip mask ROM is replaced by one-time PROM or EPROM.

The one-time PROM version can be written to once only, and is useful for short-run and multiple device-production of sets and early start-up. Also, the EPROM version allows programs to be written and rewritten, and is thus ideal for system evaluation.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μPD75238 User's Manual : IEU-731

> The μPD75P238 EPROM product does not provide a level of reliability suitable for use as a volume production product for users' devices. The EPROM product should be used solely for function evaluation in experiments of preproduction.

FEATURES

- o μPD75238 pin compatible
- o On-chip PROM: 32640 × 8
- o On-chip RAM: 1024 × 4
- o High-voltage display outputs
  - . S0 to S8 & T0 to T9 : Internal pull-down resistors
  - . S9, S16 to S23 & T10 to T15: Open-drain
- o Drive capability in same supply voltage range as mask version μPD75238 (2.7 to 6.0 V)
- o Ports 4 & 5: No pull-up resistor
- o Port 7: No pull-down resistor

Note No internal pull-up and pull-down resistor function by mask option.

USE

VCR, Audio-visual, ECR, Microwave oven

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM	Quality Grade
μPD75P238GJ-5BG	94-pin plastic QFP(□20 mm)	One-time PROM	Standard
μPD75P238KF	94-pin ceramic WQFN	EPROM	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

This manual describes common parts of One-time PROM and EPROM products as PROM.

The information in this document is subject to change without notice.

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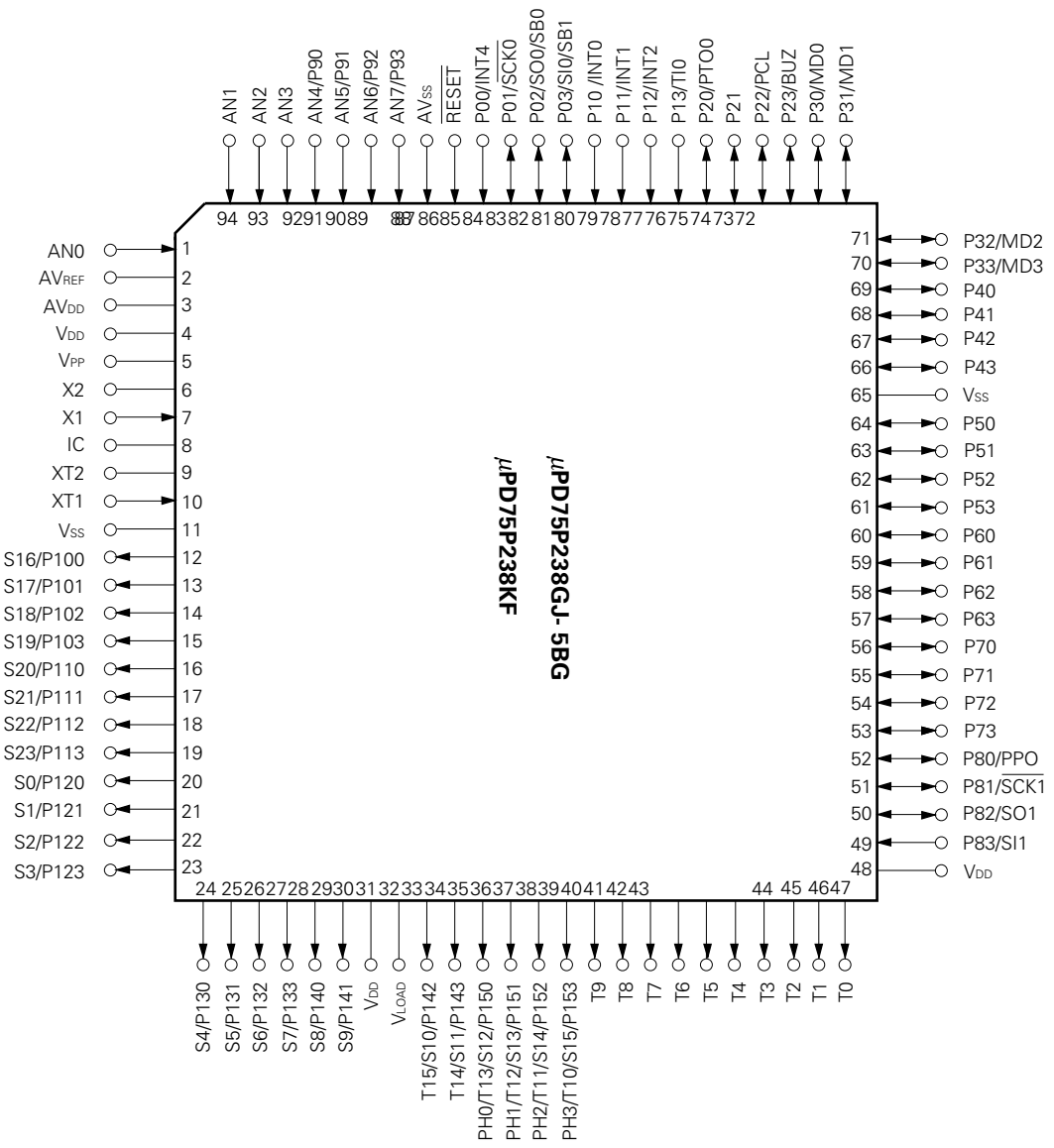
The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)



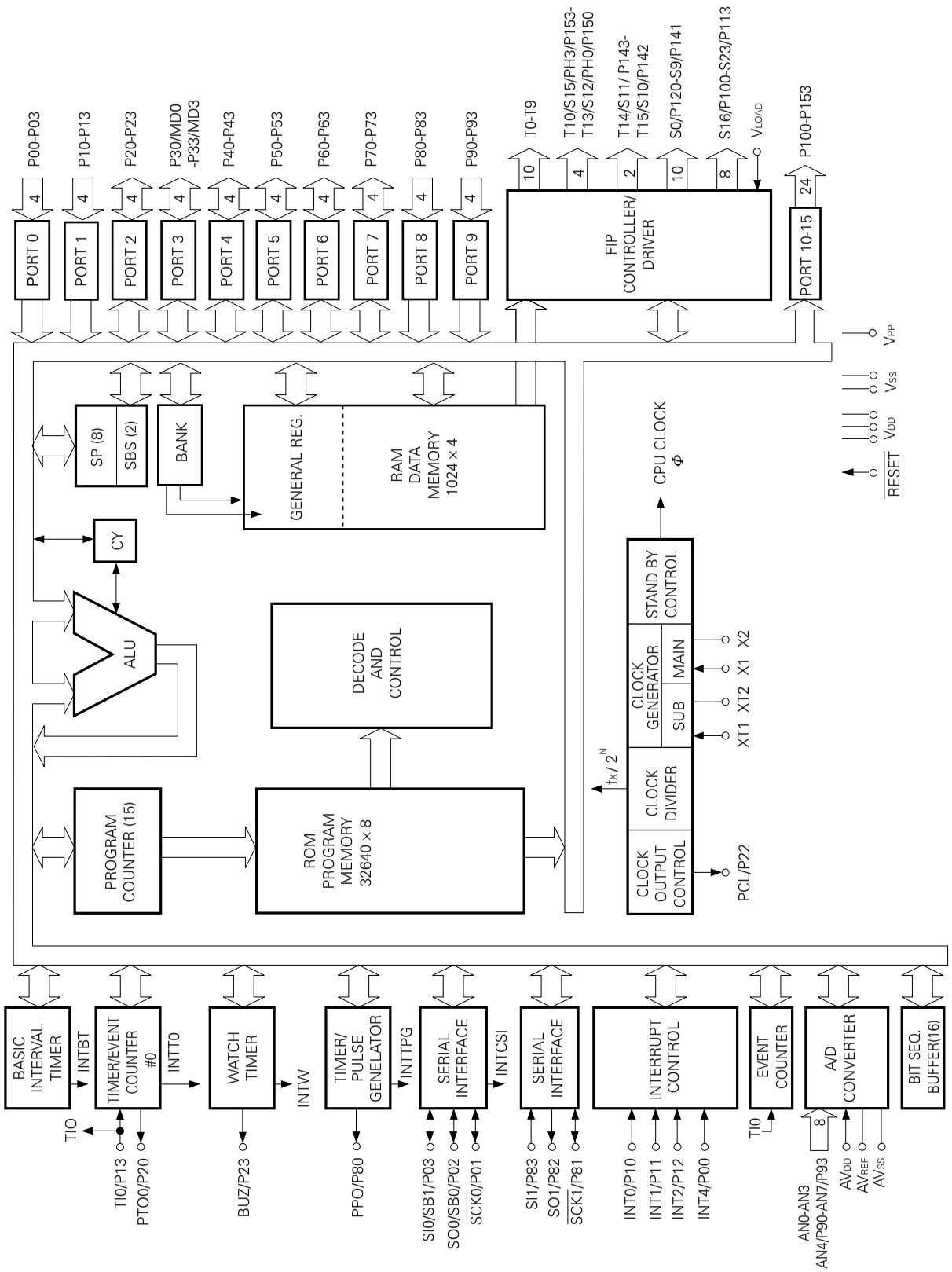
Note Ensure that power is supplied to the V_{DD} and V_{SS} pins (pins 4, 11, 30, 48, and 65).

Remarks IC (Internally Connected) pins should be connected directly to V_{SS}.

PIN NAME

P00 to P03	:	Port0	$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock I/O 0, 1
P10 to P13	:	Port1	SO0, SO1	:	Serial Data Output 0, 1
P20 to P23	:	Port2	SI0, SI1	:	Serial Data Input 0, 1
P30 to P33	:	Port3	SB0, SB1	:	Serial Bus I/O 0, 1
P40 to P43	:	Port4	INT0, INT1, INT4	:	External Vectored Interrupt Input 0, 1, 4
P50 to P53	:	Port5	INT2	:	External Test Input 2
P60 to P63	:	Port6	PPO	:	Programmable Pulse Output
P70 to P73	:	Port7	TI0	:	Timer Input 0
P80 to P83	:	Port8	PTO0	:	Programmable Timer Output 0
P90 to P93	:	Port9	BUZ	:	Buzzer Clock
P100 to P103	:	Port10	PCL	:	Programmable Clock Output
P110 to P113	:	Port11	AN0 to AN7	:	Analog Input 0 to 7
P120 to P123	:	Port12	AV_{REF}	:	Analog Reference Voltage
P130 to P133	:	Port13	AV_{DD}	:	Analog V_{DD}
P140 to P143	:	Port14	AV_{SS}	:	Analog V_{SS}
P150 to P153	:	Port15	X1, X2	:	Main System Clock Oscillation 1, 2
PH0 to PH3	:	PortH	XT1, XT2	:	Subsystem Clock Oscillation 1, 2
T0 to T15	:	Digit Output	$\overline{RESET}$	:	Reset
S0 to S23	:	Segment Output	V_{PP}	:	Programming Power Supply
V_{DD}	:	Positive Power Supply	MD0 to MD3	:	Mode Selection 0 to 3
V_{SS}	:	Ground	IC	:	Internally Connected
V_{LOAD}	:	Power Supply for FIP Driver			

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	After Reset	Input/Output Circuit Type*1
P00	Input	INT4	4-bit input port (PORT0). Internal pull-up resistor specification by software is possible for P01 to P03 as a 3-bit unit.	×	Input	Ⓑ
P01		$\overline{\text{SCK0}}$				Ⓕ – A
P02		SO0/SB0				Ⓕ – B
P03		SI0/SB1				Ⓜ – C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ – C
P11		INT1	4-bit input port (PORT1). Internal pull-up resistor specification by software is possible as a 4-bit unit.			
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT2). Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E – B
P21		—				
P22		PCL				
P23		BUZ				
P30 to P33 *2	Input/output	MD0 to MD3	Programmable 4-bit input/output port (PORT3). Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E – C
P40 to P43 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT4). Data input/output pins for program memory write/verify (low-order 4 bits).	○	Input	M – A
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT5). Data input/output pins for program memory write/verify (high-order 4 bits).		Input	M – A
P60 to P63	Input/output	—	Programmable 4-bit input/output port (PORT6). Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	○	Input	E – C
P70 to P73	Input/output	—	4-bit input/output port (PORT7).		Input	E

* **1.** A circle denotes Schmitt-triggerd input.
2. Direct LED drive capability

1.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	After Reset	Input/Output Circuit Type*1
P80	Input/output	PPO	4-bit input port (PORT8).	×	Input	A
P81	Input/output	$\overline{SCK1}$				Ⓕ
P82	Input/output	SO1				E
P83	Input	SI1				Ⓑ
P90 to P93	Input	AN4 to AN7	4-bit input port (PORT9).	×	Input	Y – A
P100 to P103	Output	S16 to S19	P-ch open-drain 4-bit high-voltage output port.	○	High impedance	I – D
P110 to P113	Output	S20 to S23	P-ch open-drain 4-bit high-voltage output port.			
P120 to P123	Output	S0 to S3	P-ch open-drain 4-bit high-voltage output port. Internal pull-down resistors.	○	V_{LOAD} level	I – E
P130 to P133	Output	S4 to S7	P-ch open-drain 4-bit high-voltage output port. Internal pull-down resistors.			I – E
P140	Output	S8	P-ch open-drain 4-bit high-voltage output port. Internal pull-down resistor on P140 only.	○	V_{LOAD} level	I – E
P141		S9			High impedance	I – D
P142*2		S10/T15				
P143*2		S11/T14				
P150*2	Output	S12/T13/PH0	P-ch open-drain 4-bit high-voltage output port.			I – D
P151*2		S13/T12/PH1				
P152*2		S14/T11/PH2				
P153*2		S15/T10/PH3				
PH0	Output	S12/T13/P150	P-ch open-drain 4-bit high-voltage output port.	×	High impedance	I – D
PH1		S13/T12/P151				
PH2		S14/T11/P152				
PH3		S15/T10/P153				

* **1.** A circle denotes Schmitt-triggerd input.
2. Direct LED drive capability.

1.2 NON-PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function		After Reset	Input/Output Circuit Type*
PPO	Output	P80	Timer/pulse generator pulse output pin.		Input	A
TI0	Input	P13	External event pulse input pin for timer/event counter #0 or event counter #1.		——	Ⓑ – C
PTO0	Output	P20	Timer/event counter output pin.		Input	E – B
PCL	Output	P22	Clock output pin.		Input	E – B
BUZ	Output	P23	Fixed-frequency output pin (for buzzer or system clock trimming use).		Input	E – B
$\overline{SCK0}$	Input/output	P01	Serial clock input/output pin.		Input	Ⓕ – A
SO0/SB0	Input/output	P02	Serial data output pin. Serial bus input/output pin.		Input	Ⓕ – B
SI0/SB1	Input/output	P03	Serial data input pin. Serial bus input/output pin.		Input	Ⓜ – C
INT4	Input	P00	Edge-detected vectored interrupt input pin (either rising or falling edge detection).		——	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input pin (detected edge selectable).	Clocked	——	Ⓑ – C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge-detection testable input pin (rising edge detection).	Asynchronous	——	Ⓑ – C
$\overline{SCK1}$	Input/output	P81	Serial clock input/output pin.		Input	Ⓕ
SO1	Output	P82	Serial data output pin.		Input	E
SI1	Input	P83	Serial data input pin.		Input	Ⓑ
AN0 to AN3	Input	——	A/D converter analog input pin.		——	Y
AN4 to AN7		P90 to P93				Y – A
AV_{REF}	Input	——	A/D converter reference voltage input pin.		——	Z
AV_{DD}	——	——	A/D converter power supply pin.		——	——
AV_{SS}	——	——	A/D converter reference GND potential pin.		——	——
X1, X2	Input	——	Main system clock oscillation crystal/ceramic resonator input. When an external clock is used, the clock is input to X1 and the inverted clock to X2.		——	——
XT1	Input	——	Subsystem clock oscillation crystal resonator input. When an external clock is used, the clock is input to XT1 and XT2 is left open.		——	——
XT2	——					
$\overline{RESET}$	Input	——	System reset input pin.		——	Ⓑ
MD0 to MD3	Input	P30 to P33	Mode selection pin for program memory write/verify.		——	E – C
IC	——	——	Internally Connected . Connect to V_{SS} directly.		——	—— ★
V_{PP}	——	——	Program voltage application pin for program memory write/verify . Connected to V_{DD} in normal operation. Applies +12.5 V in program memory write/verify.		——	——

* A circle denotes Schmitt-triggerd input.

1.2 NON-PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	Input/Output Circuit Type
V_{DD} (3 pins)	—	—	Positive power supply pins. Apply +6 V in PROM write/verify.	—	—
V_{SS} (2 pins)	—	—	Ground potential pin.	—	—
V_{LOAD}	—	—	FIP controller/driver pull-down resistor connection/ power supply pin.	—	I – D
T0 to T9 *	Output	—	Digit output high-voltage large large-current output pins.	V_{LOAD} level	I – E
T10/S15 to T13/S12		PH3/P153 to PH0/P150	Digit/segment output dual-function high-voltage large-current output pins. Unused pins usable as Port H. Usable as Port 15 in static mode.	High impedance	I – D
T14/S11		P143	Digit/segment output dual-function high-voltage large-current output pin. Usable as Port 14 in static mode.	High impedance	I – D
T15/S10		P142			
S0 to S3 *		P120 to P123	Segment high-voltage output pins. Usable as Port 12 to Port 14 in static mode.	V_{LOAD} level	I – E
S4 to S7 *		P130 to P133		V_{LOAD} level	I – E
S8 *		P140		V_{LOAD} level	I – E
S9		P141		High impedance	I – D
S16 to S19		P100 to P103	Segment high-voltage output pins. Usable as Port 10 & Port 11 in static mode.	High impedance	I – D
S20 to S23		P110 to P113		High impedance	I – D

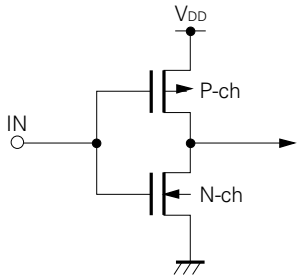
* Internal pull-down resistor

1.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuits for each of the pins are shown in Fig. 1-1 in partially simplified form.

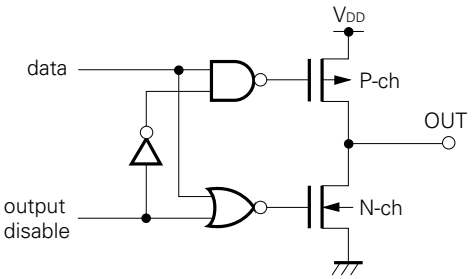
Fig. 1-1 Pin Input/Output Circuits (1/3)

TYPE A



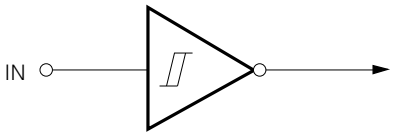
CMOS Standard Input Buffer

TYPE D



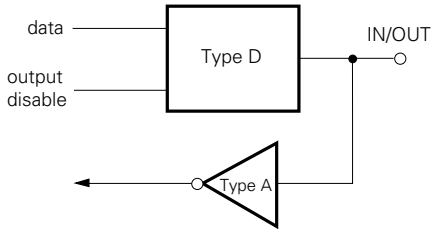
Push-Pull Output with High Impedance Output Capability (P-ch and N-ch both OFF)

TYPE B



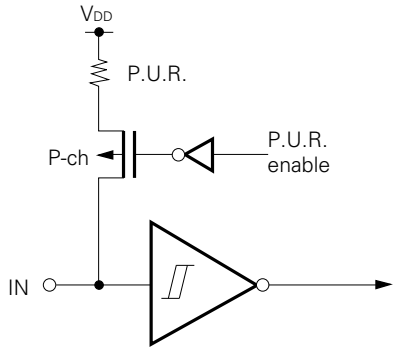
Schmitt-Triggered Input with Hysteresis Characteristics

TYPE E



Input/Output Circuit Composed of Type D Push-Pull Output and Type A Input Buffer

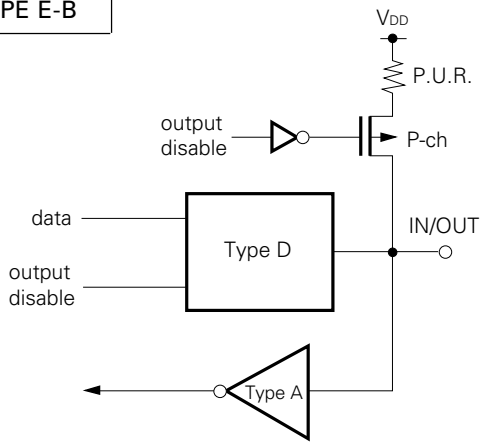
TYPE B-C



P.U.R. : Pull-Up Resistor

Schmitt-Triggered Input with Hysteresis Characteristics

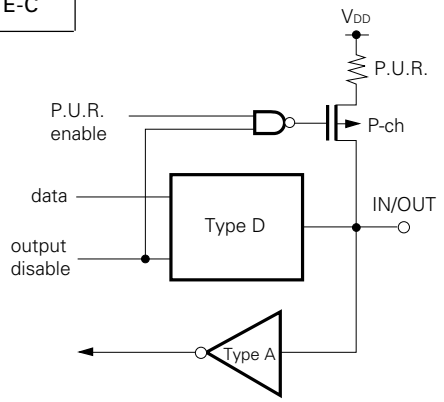
TYPE E-B



P.U.R.:Pull-Up Resistor

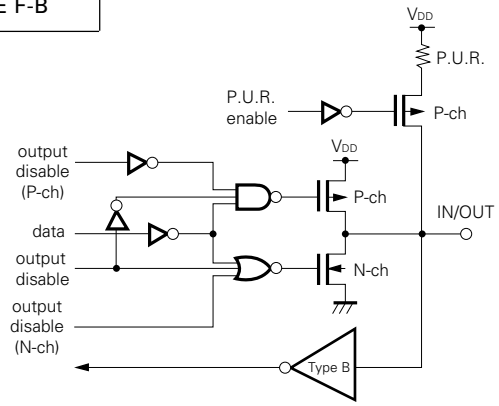
Fig. 1-1 Pin Input/Output Circuits (2/3)

TYPE E-C



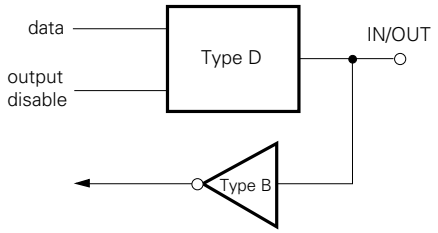
P.U.R.:Pull-Up Resistor

TYPE F-B



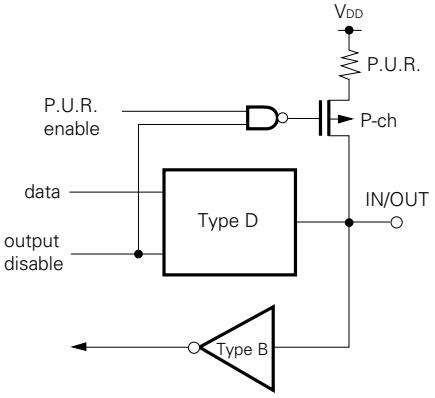
P.U.R.:Pull-Up Resistor

TYPE F



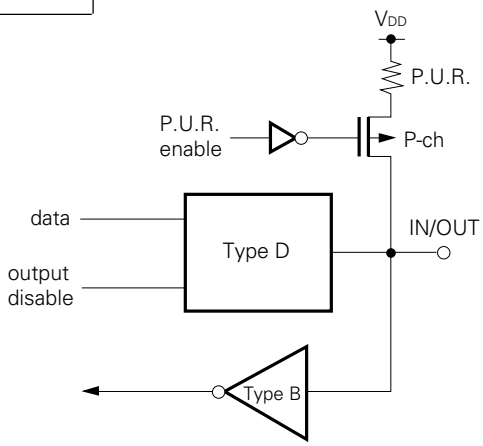
Input /Output Circuit Composed of Type D Push-Pull Output and Type B Schmitt-Triggered Input

TYPE F-C



P.U.R.:Pull-Up Resistor

TYPE F-A



P.U.R.:Pull-Up Resistor

TYPE I-D

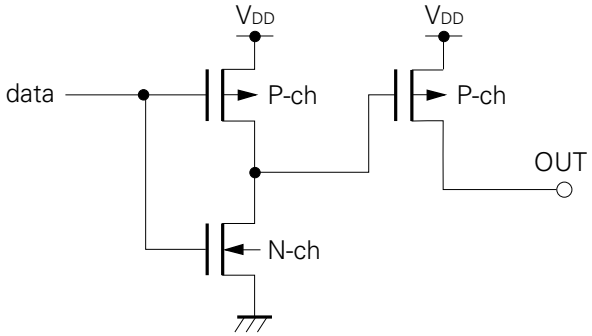
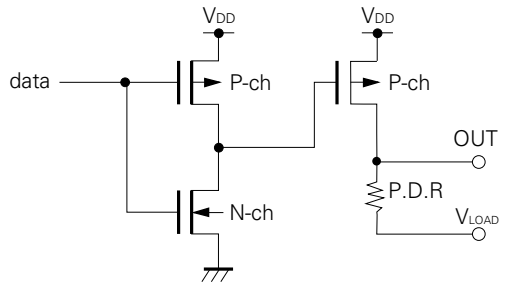


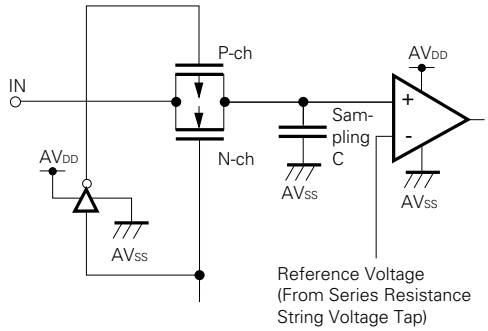
Fig. 1-1 Pin Input/Output Circuits (3/3)

TYPE I-E

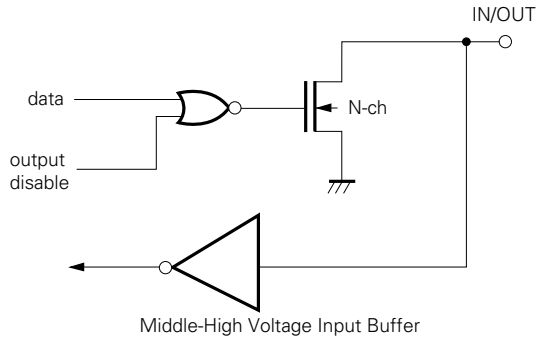


P.D.R: Pull-Down Resistor

TYPE Y

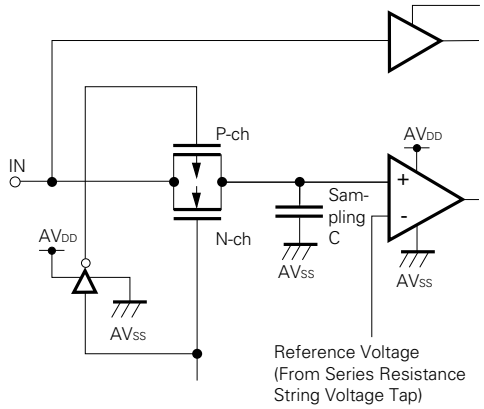


TYPE M-A

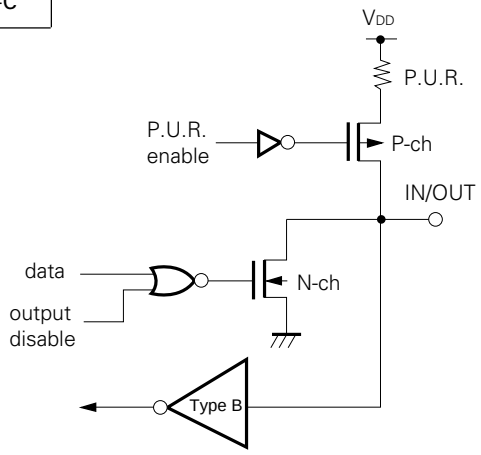


P.U.R: Pull-Up Resistor

TYPE Y-A

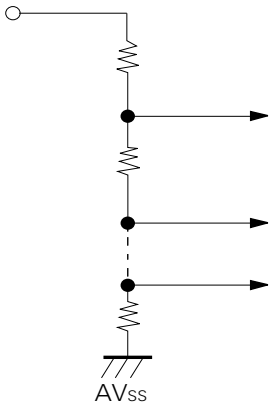


TYPE M-C



P.U.R: Pull-Up Resistor

TYPE Z



1.4 DISPOSITION OF UNUSED PIN

Table 1-2 Recommended Commection of Unused Pins (1/2)

Pin	Recommended Connection
P00/INT4	Connect to V_{SS}.
P01/$\overline{SCK0}$	Connect to V_{SS} or V_{DD}.
P02/SO0/SB0	
P03/SI1/SB1	
P10/INT0 to P12/INT2	Connect to V_{SS}.
P13/TI0	
P20/PTO0	Input state : Connect to V_{SS} or V_{DD}. Output state : Leave open.
P21	
P22/PCL	
P23/BUZ	
P30 to P33	
P40 to P43	
P50 to P53	
P60 to P63	
P70 to P73	
P80 to PPO	Connect to V_{SS} or V_{DD}.
P81 to $\overline{SCK1}$	
P82/SO1	
P83/SI1	
P90/AN4 to P93/AN7	Connect to V_{SS}.

Table 1-2 Recommended Commection of Unused Pins (2/2)

Pin	Recommended Connection
P100/S16 to P103/S19	Leave open.
P110/S20 to P113/S23	
P120 to P123	
P130 to P133	
P140 to P143	
P150 to P153	
AN0 to AN3	Connect to V_{SS}.
AV_{REF}	
AV_{DD}	Connect to V_{DD}.
AV_{SS}	Connect to V_{SS}.
XT1	Connect to V_{SS} or V_{DD}.
XT2	Leave open.
V_{LOAD}	Connect to V_{SS} or leave open.
IC	Connect to V_{SS}. ★

2. DIFFERENCES BETWEEN μPD75P238 AND μPD75238

The μPD75P238 is a product with the program memory of the μPD75238 using on-chip mask ROM replaced by one-time PROM or EPROM. Table 2-1 shows differences between μPD75P238 and μPD75238. The differences between these products must be thoroughly checked when, for example, switching from use of PROM for application system debugging and reproduction to use of a mask ROM product for volume production.

For details of CPU function and on-chip hardware, refer to the document "**μPD75238 User's Manual" (IEU-731)**.

Table 2-1 Differences between μPD75P238 and μPD75238

Parameter \ Product Name		μPD75238	μPD75P238
ROM		Mask ROM 32K × 8	One-time PROM, EPROM 32K × 8
RAM		1K × 4	
FIP controller/ driver	No. of segments	9 to 24	
	No. of digits	9 to16	
Pull-up resistors	Ports 4 & 5	Mask option	No
Pull-down resistors	Port 7		No
	S0 to S8		On-chip
	S9		No
	S16 to S23		No
	T0 to T9		On-chip
	T10 to T15		No
Pin connection	Pin 5	V_{DD}	V_{PP}
	Pins 70 to 73	P30 to P33	P30/MD0 to P33/MD3
★ Electrical specifications		The mask ROM products and PROM products have different consumption currents, operating temperature range etc. See the Electrical Specifications section in the relevant Data Sheet for details.	
Operating supply voltage range		2.7 to 6.0 V	
Subsystem clock feedback resistor		Mask option	On-chip
Package		94-pin plastic QFP (□20 mm)	94-pin plastic QFP (□20 mm) 94-pin ceramic WQFN
★ Others		The mask ROM products and PROM products have different circuit scales and mask layouts, and therefore differ in terms of noise resistance and noise radiation.	

★ **Note Noise resistance and noise radiation differs between the PROM products and mask ROM products. When investigating a switch from preproduction to volume production, throughout evaluation should be carried out with the mask ROM CS product (not the ES product).**

3. PROGRAM MEMORY (PROM)

The program memory is PROM with a 32640 × 8-bit configuration wich stores program and table tata etc.

The program memory is addressed by the program counter. In addition, table data can be referenced by a table referencing instruction (MOVT).

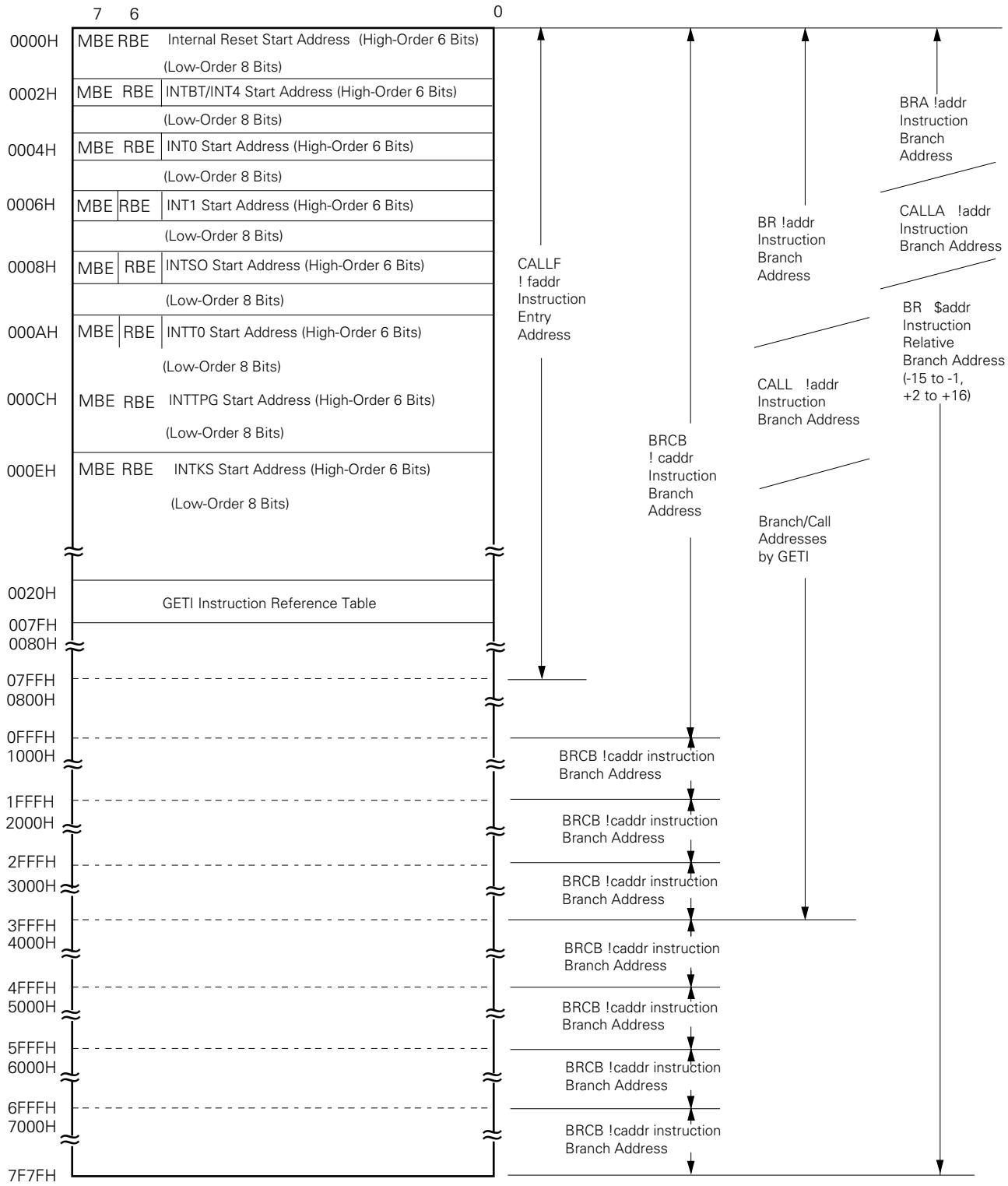
The rage of address to which branch instructions and subroutine call instructions and subroutine call instructions and subroutine call instructions can branch is shown in Fig. 3-1. The entire space comprising 0000H to 7F7FH can be directly branched to by the entire-space branch instruction (BRA !addr1) and the entire-space call instruction (CALLA !addr1). The relative branch instruction (BR $addr) allows branching to addresses [PC contents –15 to –1 and +2 to +16] irrespective of block boundaries.

In addition, the following addresses are specially allocated (except for 0000H and 0001H, the entire area can be used as ordinary program memory).

- Addresses 0000H & 0001H
  Vector table to which the program start address and MBE & RBE set value upon $\overline{\text{RESET}}$ input are written.
  Reset servicing can be started from any address in the 16K (000H to 3FFFH).
- Addresses 0002H to 000FH
  Vector table to which the program start address and MBE & RBE set value for the various vectore interrupts are written. Interrupt servicing can be started from any address in the 16K space (0000H to 3FFFH).
- Addresses 0020H to 007FH
  Table area referenced by GETI instruction*.

* The GETI instruction allows any 2- or 3-byte instruction or any two 1-byte instructions to be implemented as 1 byte, and is used to reduce the number of program steps.

Fig. 3-1 Program Memory Map



Note The above interrupt vector start addresses are 14-bit, and thus should be set in the 16K space (0000H to 3FFFH).

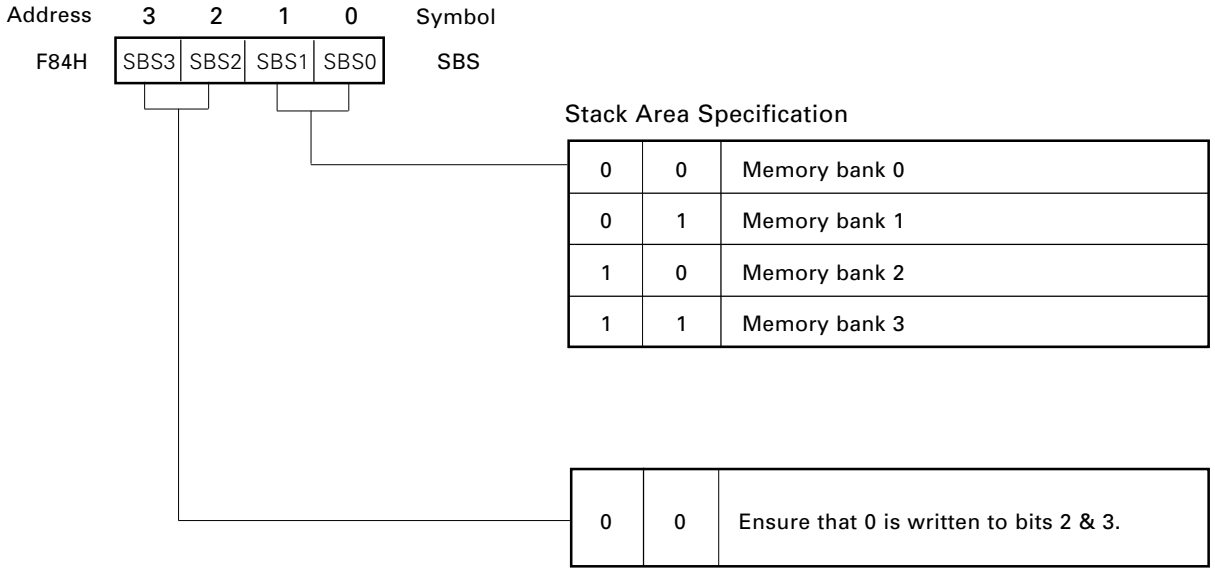
Remarks In addition to the above, branching is possible with the BR PCDE and BR PCXA instructions to addresses with the low-order 8 bits only of the PC modified.

4. STACK BANK SELECTION REGISTER (SBS)

The stack bank selection register specifies one memory bank from memory banks 0 to 3 as the stack area.Its format is shown in Fig. 4-1.

The stack bank selection register is set by a 4-bit memory manipuration instruction. On $\overline{\text{RESET}}$ input bit only is set to "1" and the remaining bits are undefined. Therefore this register must always be initialized to 00××B* at the start of a program.

Fig. 4-1 Stack Bank Selection Register Format



Note After $\overline{\text{RESET}}$ input a subroutine call instruction and interrupt enabling instruction should be executed after setting the stack bank selection register.

* ×× should be set to the desired value.

5. PROGRAM MEMORY WRITE AND VERIFY OPERATIONS

The program memory incorporated in the μPD75P238 is 32640 × 8-bit electrically writable PROM. Write/verify operations on this PROM are executed using the pins shown in the table below. Address updating is performed by means of clock input from the X1 pin rather than by address input.

Table 5-1 Pins Used for Program Memory Write/Verify

Pin Name	Function
V_{PP}	Voltage applecation pin for program memory write/verify (normally V_{DD} potential).
X1, X2	Address update clock input for program memory write/verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pin for program memory write/verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pin for progrm memory write/verify.
V_{DD}	Supply voltage application pin. Applies 2.7 to 6.0 V in normal operation, and 6 V for program memory write/verify.

Note 1. Pins not used in a program memory write/verify operation are handled as follows:

Ports 0 to 2, ports 6 to 15
T0 to T9, AN0 to AN3, XT1 ..... **Connect to GND**
V_{LOAD}, AV_{REF}, AV_{SS}, $\overline{RESET}$

AV_{DD} ..... **Connect to V_{DD}**

XT2 ..... **Leave open**

2. **On the μPD75P238KF which is equipped with an erase window the shading cover film should be attached except when performing EPROM erasure.**
3. **Since the μPD75P238GJ one-time PROM version is not provided with an erase window, program memory contents cannot be erased.**

5.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD75P238 enters the program memory write/verify mode. This mode comprises one of the operating modes shown in Table 5-2 according to the setting of pins MD0 to MD3.

Table 5-2 Program Memory Write/Verify Operating Modes

Operating Mode Setting						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+ 12.5 V	+ 6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

Remarks ×: L or H

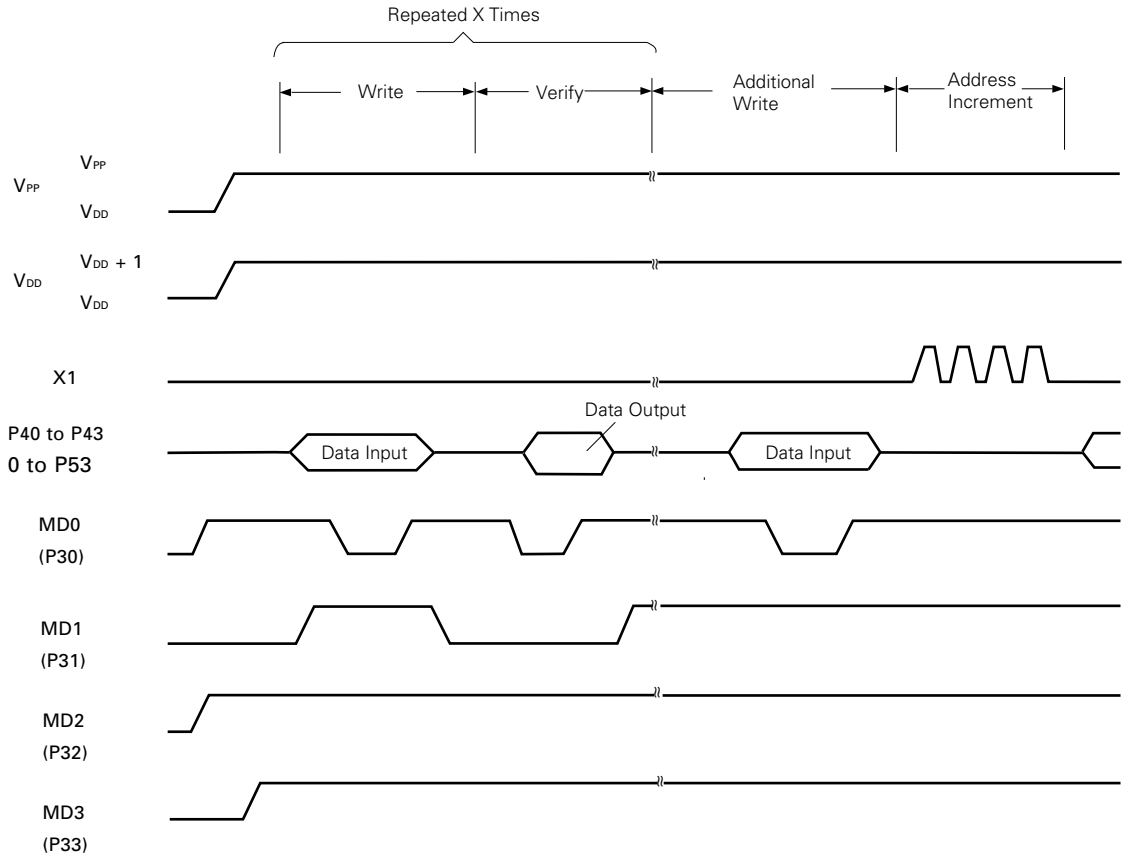
5.2 PROGRAM MEMORY WRITE PROCEDURE

The procedure for writing to program memory is as shown below, allowing high-speed writing.

(1) Unused pins are connected to V_{SS}. The X1 pin is driven low.
(2) 5 V is supplied to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) Program memory address zero-clear mode.
(5) 6V is supplied to V_{DD}, 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Data is written in 1 ms write mode.
(8) Program inhibit mode.
(9) Verify mode. If write is successful go to (10), otherwise repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) × 1 ms additional writes.
(11) Program inhibit mode.
(12) Program memory address is updated (+1) by inputting 4 pulses to the X1 pin.
(13) Steps (7) to (12) are repeated until the last address.
(14) Program memory address zero-clear mode.
(15) V_{DD} / V_{PP} pin voltage is changed to 5 V.
(16) Power-off.

Steps (2) to (12) of this procedure are shown in Fig. 5-1.

Fig. 5-1 Program Memory Write Timing



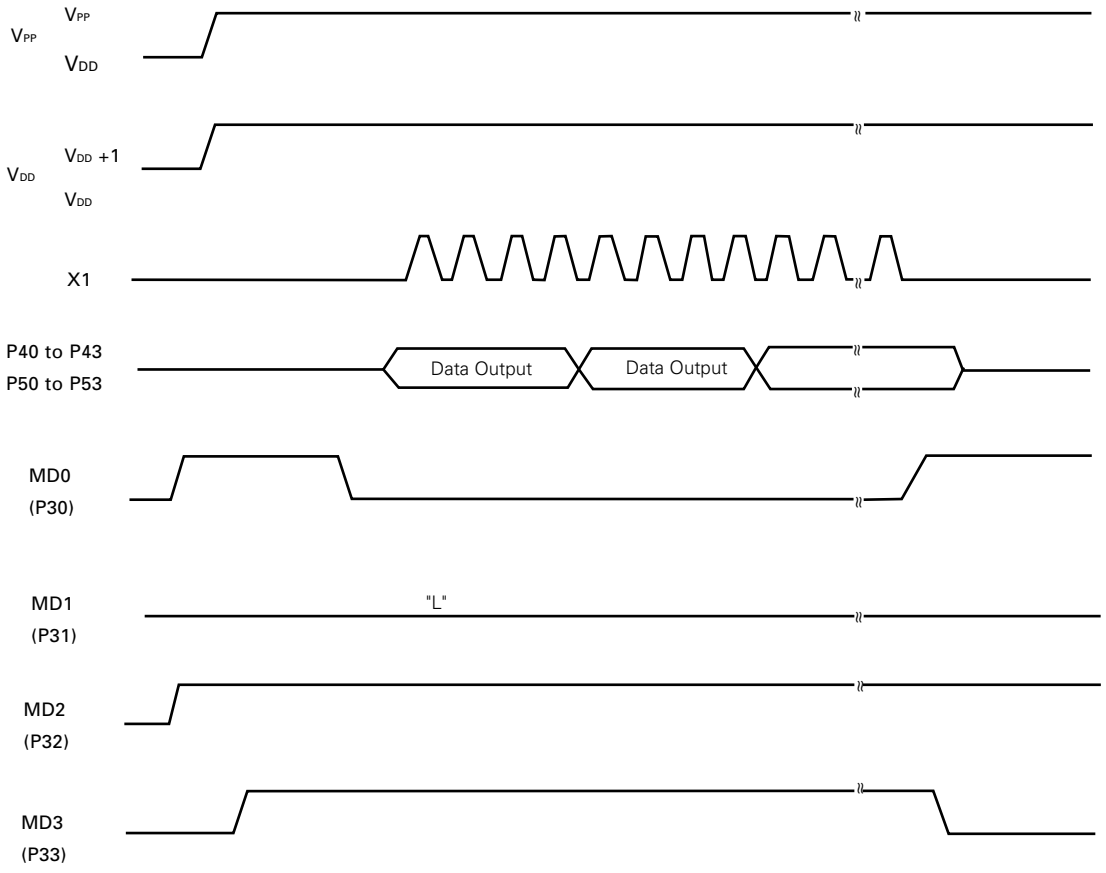
5.3 PROGRAM MEMORY READ PROCEDURE

μPD75P238 program memory contents can be read using the following procedure. Reading is performed in verify mode.

(1) Unused pins are connected to V_{SS}. The X1 pin is driven low.
(2) 5 V is supplied to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) Program memory address zero-clear mode.
(5) 6 V supplied to V_{DD}, and 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Verify mode. When clock pulses are input to the X1 pin, data is output sequentially, one address per 4-pulse-input cycle.
(8) Program inhibit mode.
(9) Program memory address zero-clear mode.
(10) V_{DD} / V_{PP} pin voltage is changed to 5 V.
(11) Power-off.

Steps (2) to (9) of this procedure are shown in Fig. 5-2.

Fig. 5-2 Program Memory Read Timing



5.4 ERASURE (μPD75P238KF ONLY)

The Programmed data contents of the μPD75P238KF can be erased by exposure to ultraviolet light through the window in the top.

The ultraviolet wave length which effects erasure is 250 nm, and the quantity of radiation necesary for complete erasure is 15 W•s/cm^2 (ultraviolet radiation intensity x erasure time). Using a commercially available ultraviolet lamp (254 nm vavelength, 12 mW/cm^2 intensity) erasure can be accomplished in approximately 15 to 20 minutes.

Note 1. Memory contents may also be erased by prolonged exposure to direct sunlight fluorescent lighting. To protect the contents ensure that the top window is masked with the shading cover film. The shading cover film supplied with NEC's UV EPROM products should be used.

2. When carrying out erasure the distance between the ultraviolet lamp and the μPD75P238KF should normally be no greater than 2.5 cm.

Remarks A longer erasure time may be required if there is deterioration of the ultraviolet lamp, or if the package window is not clean, etc.

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{LOAD}			V_{DD} –40 to V_{DD} +0.3	V
	V_{PP}			–0.3 to +13.5	V
Input voltage	V_{I1}	Except ports 4, 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5	Open-drain	–0.3 to +11	V
Output voltage	V_O	Pins except display output pins		–0.3 to V_{DD} +0.3	V
	V_{OD}	Display output pins		V_{DD} –40 to V_{DD} +0.3	V
Output current high	I_{OH}	1 pin except display output pins		–15	mA
		S0 to S9, S16 to S23 1 pin		–15	mA
		T0 to T15 1 pin		–30	mA
		All pins except display output pins		–30	mA
		All display output pins		–120	mA
Output current low	I_{OL}*	1 pin	Peak value	30	mA
			Effective value	15	mA
		Total of port 0, 2, 3, 4	Peak value	100	mA
			Effective value	60	mA
		Total of port 5 to 8	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T_{opt}			–40 to +70	°C
Storage temperature	T_{stg}			–65 to +150	°C

* The Effective value should be calculated as follows. [Effective value] = [Peak value] × $\sqrt{\text{Duty}}$

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute ratings are not exceeded. ★

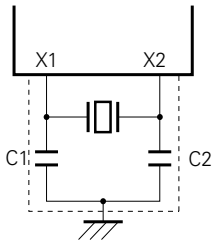
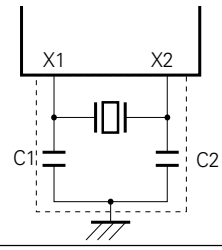
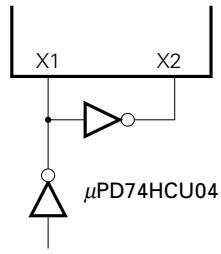
OPERATING SUPPLY VOLTAGE RANGE (Ta = –40 to +70 °C)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU***1**		***2**	6.0	V
Display controller		4.5	6.0	V
Timer/pulse generator		4.5	6.0	V
Other hardware***1**		2.7	6.0	V

*** 1.** Except the system clock oscillator, display controller and timer/pulse generator.

2. The operating power supply voltage range varies depending on the cycle time. Refer to the section describing AC characteristics.

MAIN SYSTEM CLOCK RESONATOR CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CHARACTERISTICS	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_x)***1**	V_{DD} = Oscillator voltage range	2.0		6.2	MHz
		Oscillation stabilization time***2**	After V_{DD} has reached MIN. value of oscillator voltage range.			4	ms
Crystal resonator		Oscillator frequency (f_x)***1**		2.0	4.19	6.2	MHz
		Oscillation stabilization time***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_x)***1**		2.0		6.2	MHz
		X1 input high and low level width (t_{XH}, t_{XL})		81		250	ns

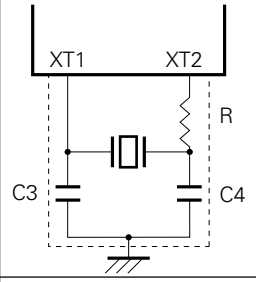
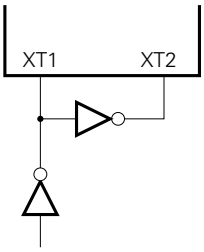
*** 1.** Oscillator frequency and input frequency indicate oscillator characteristics only. Refer to the AC characteristics for the instruction execution time.

2. Oscillation stability time is time required for oscillation to stabilize after V_{DD} has reached the MIN. value in oscillation voltage range or STOP mode has been released.

Note When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc. ★

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines caring a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CHARACTERISTICS	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT})***1**		32	32.768	35	kHz
		Oscillation stabilization time***1**	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External Clock		XT1 input frequency (f_{XT})***1**		32		100	kHz
		X1 input high and low level width (t_{XTH}, t_{XTL})		5		15	μs

*** 1.** Oscillator frequency and input frequency indicate oscillator characteristics only. Refer to the AC characteristics for the instruction execution time.

2. Oscillation stability time is time required for oscillation to stabilize after V_{DD} has reached the MIN. value in oscillation voltage range.

★ **Note When subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.**

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines caring a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system, clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

CAPACITANCE (Ta =25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz 0 V for pins except measured pins			15	pF
Output capacitance (Output except display output)	C_O				15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance (Display output)	C_O				35	pF

RECOMMENDED OSCILLATOR CONTANTS

MAINSYSTEMCLOCK : CERAMIC RESONATOR (Ta = – 40 to + 85 °C)

MAUNFACTURER	PRODUCT NAME	FREQUENCY (MHz)	RECOMMENDED OSCILLATOR CONSTANTS(pF)		OSCILLATOR VOLTAGE RANGE(V)		REMARKS
			C1	C2	MIN.	MAX.	
Murata Mfg.	CSA2.0MG	2.0	30	30	2.7	6.0	
	CST2.0MG		–	–			On-chip capacitor product
	CSA2.5MG093	2.5	30	30			
	CST2.5MGW093		–	–			On-chip capacitor product
	CSA4.19MGU	4.19	30	30			
	CST4.19MGWU		–	–			On-chip capacitor product
	CSA2.5MG	2.5	30	30	3.0	6.0	
	CST2.5MGW		–	–			On-chip capacitor product
	CSA4.19MG	4.19	30	30	3.3	6.0	
	CST4.19MGW		–	–			On-chip capacitor product
	CSA6.0MG	6.00	30	30	4.0	6.0	
	CST6.0MGW		–	–			On-chip capacitor product

MAIN SYSTEM CLOCK : CRYSTAL RESONATOR (Ta = – 20 to + 70 °C)

MAUNFACTURER	PRODUCT NAME	FREQUENCY (MHz)	RECOMMENDED OSCILLATOR CONSTANTS(pF)		OSCILLATOR VOLTAGE RANGE(V)		REMARKS
			C1	C2	MIN.	MAX.	
Kinseki, Ltd.	HC-49/U-S	3.072 to 6.000	22	22	4.0	6.0	

DC CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V) (1/3)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	All ports and pins except those listed below.			0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Port 0, 1, $\overline{\text{RESET}}$, P81, P83			0.8 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, XT1			V_{DD} –0.4		V_{DD}	V
	V_{IH4}	Port 7	V_{DD} = 4.5 to 6.0 V		0.65 V_{DD}		V_{DD}	V
					0.7 V_{DD}		V_{DD}	V
	V_{IH5}	Port 4, 5	Open-drain		0.7 V_{DD}		10	V
Input voltage low	V_{IL1}	All ports and pins except those listed below.			0		0.3 V_{DD}	V
	V_{IL2}	Port 0, 1, $\overline{\text{RESET}}$, P81, P83			0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1			0		0.4	V
Output voltage high	V_{OH}	All output pins, except port 4, 5 and P03	V_{DD} = 4.5 to 6.0 V	I_{OH} = –1 mA	V_{DD} –1.0			V
			V_{DD} = 2.7 to 6.0 V	I_{OH} = –100 μA	V_{DD} –0.5			V
Output voltage low	V_{OL}	Ports 3, 4, 5	V_{DD} = 4.5 to 6.0 V	I_{OH} = 15 mA		0.4	2.0	V
		All output pins	V_{DD} = 4.5 to 6.0 V	I_{OL} = 1.6 mA			0.4	V
			V_{DD} = 2.7 to 6.0 V	I_{OL} = 400 μA			0.5	V
		SB0, SB1	Open-drain pull-up resistor ≥ 1 kΩ				0.2 V_{DD}	V
Input leakage current high	I_{LIH1}	All ports and pins except those listed below.	V_{IN} = V_{DD}				3	μA
	I_{LIH2}	X1, X2, XT1					20	μA
	I_{LIH3}	Ports 4, 5	V_{IN} = 10 V				20	μA
Input leakage current low	I_{LIL1}	All ports and pins except those listed below.	V_{IN} = 0 V				–3	μA
	I_{LIL2}	X1, X2, XT1					–20	μA

DC CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V) (2/3)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Output leakage current high	I_{LOH1}	All ports and pins except those listed below.	$V_{OUT} = V_{DD}$				3	μA
	I_{LOH2}	Port 4, 5	V_{OUT} = 10 V				20	μA
Output leakage current low	I_{LOL1}	All ports and pins except those listed below.	V_{OUT} = 0 V				–3	μA
	I_{LOL2}	Display output	$V_{OUT} = V_{LOAD} = V_{DD}$ – 35 V				–10	μA
Display output current	I_{OD}	S0 to S9, S16 to S23	V_{DD} = 4.5 to 6.0 V $V_{OD} = V_{DD}$ – 2 V		–3	–5.5		mA
		T0 to T15			–15	–22		mA
On-chip pull-down resistor (Mask option)	R_L	Display output	$V_{OD} – V_{LOAD}$ = 35 V		25	50	135	kΩ
On-chip pull-up resistor	R_{V1}	Port 0, 1, 2, 3, 6 (Except P00) V_{IN} = 0 V	V_{DD} = 5 V ± 10%		15	40	80	kΩ
			V_{DD} = 3 V ± 10%		30		300	kΩ
Power supply current***1**	I_{DD1}	6MHz crystal oscillation C1 = C2 = 22 pF***4**	Operating mode	V_{DD} = 5V ±10%***2**		9	18	mA
				V_{DD} = 3 V ±10%***3**		1	3	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10%		900	2700	μA
				V_{DD} = 3 V ±10%		300	900	μA
	I_{DD1}	4.19MHz crystal oscillation C1 = C2 = 22 pF***4**	Operating mode	V_{DD} = 5 V ±10%***2**		5	15	mA
				V_{DD} = 3 V ±10%***3**		0.9	2.7	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10%		600	1800	μA
				V_{DD} = 3 V ±10%		200	600	μA

***** **1.** Current to the on-chip pull-down resistor (pull-up) and power-on reset circuit (mask option) is not included.

2. When the processor clock control register (PCC) is set to 0011 and is operated at high-speed mode.

3. When the PCC register is set to 0000 and is operated in the low-speed mode.

4. Includes the case where the subsystem clock oscillating.

DC CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V) (3/3)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Power supply current*1	I_{DD3}	32 kHz crystal oscillation*2	Operating mode	V_{DD} = 3 V ±10%		100	300	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10%		20	60	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10%			0.5	20	μA
			V_{DD} = 3 V ±10%			0.3	10	μA
				Ta = 25°C			5	μA
	I_{DD6}	32 kHz crystal oscillation*2	STOP mode	V_{DD} = 3 V ±10%		5	15	μA

* **1.** Current to the on-chip pull-down resistor (pull-up) and power-on reset circuit (mask option) is not included.

2. When the system clock control register (SCC) is set to 1001 and is operated with the subsystem clock with main system clock oscillation stopped.

A/D CONVERTER CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V, 2.7 ≤ AV_{DD} ≤ V_{DD})

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Resolution				8	8	8	bit
Absolute accuracy*1		2.5 V ≤ AV_{REF} ≤ V_{DD}	–10 ≤ Ta ≤ +70°C			±1.5	LSB
			–40 ≤ Ta < –10°C			±2.0	
Conversion time	t_{CONV}	*2				168/f_X	μs
Sampling time	t_{SAMP}	*3				44/f_X	μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	I_{AREF}				1.0	2.0	mA

* **1.** Absolute accuracy except quantization error (±1/2 LSB).

2. Time from execution of conversion start instruction to EOC = 1 (28.0 μs when f_X = 6.0 MHz, 40.1 μs when f_X = 4.19 MHz)

3. Time from execution of conversion start instruction to the end of sampling (7.33 μs when f_X = 6.0 MHz, 10.5 μs when f_X = 4.19 MHz)

AC CHARACTERISTICS (Ta = –40 to +70 °C, V_{DD} = 2.7 to 6.0 V)

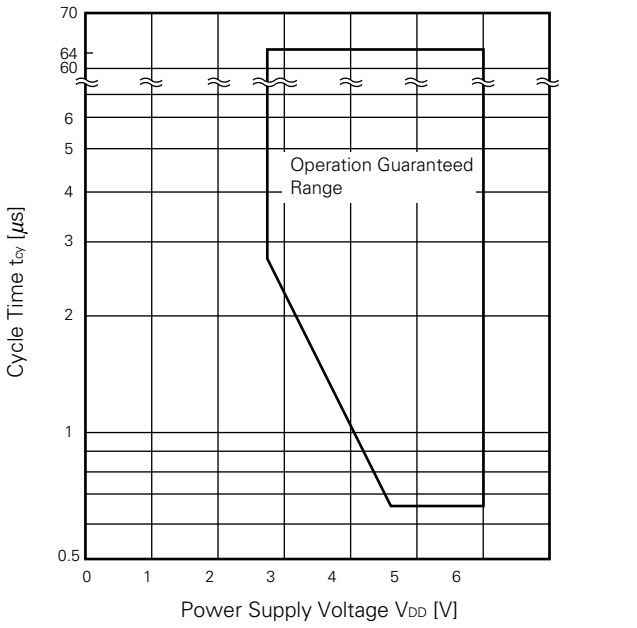
(1) Basic Operation

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = one machine cycle)***1**	t_{CY}	Operation with main system clock	V_{DD} = 4.75 to 6.0 V	0.67		64	μs
				2.6		64	μs
		Operation with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high and low-level widths	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
$\overline{\text{RESET}}$ low level widths	t_{RSL}			10			μs

*** 1.** CPU clock (Φ) cycle time is determined by the oscillator for frequency of the connected oscillator, the system clock control register (SCC) and processor clock control register (PCC). The cycle time t_{CY} characteristics for supply voltage V_{DD} when the main system clock is in operation is shown on the right.

2. $2t_{CY}$ or $128/f_X$ is set by interrupt mode register (IM0) setting.

t_{CY} vs V_{DD}
(When main system clock is in operation)



(2) Serial Transfer Operation

(a) 2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V	f_X = 6.0 MHz	1340			ns
			f_X = 4.19 MHz	1600			ns
			f_X = 6.0 MHz	2680			ns
			f_X = 4.19 MHz	3800			ns
$\overline{SCK}$ high and low level widths	t_{KL1} t_{KH1}	V_{DD} = 4.5 to 6.0 V		(t_{KCY1}/2) -50			ns
				(t_{KCY1}/2) -150			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	R_L = 1 kΩ , C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

* R_L and C_L denote load resistor and load capacitance of SO output line.

(b) 2-Wired and 3-Wired Serial I/O Modes ($\overline{SCK}$ ... External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high and low level widths	t_{KL2} t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	R_L = 1 kΩ , C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L denote load resistor and load capacitance of SO output line.

(c) SBI Mode ($\overline{SCK}$ ... Internal clock output (Master))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V	f_X = 6.0 MHz	1340			ns
			f_X = 4.19 MHz	1600			ns
			f_X = 6.0 MHz	2680			ns
			f_X = 4.19 MHz	3800			ns
$\overline{SCK}$ high and low level widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low level widths	t_{SBL}			t_{KCY3}			ns
SB0, 1 high level widths	t_{SBH}			t_{KCY3}			ns

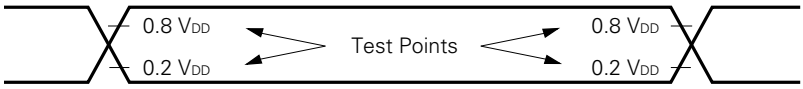
* R_L and C_L denote load resistor and load capacitance of SO output lines.

(d) SBI Mode ($\overline{SCK}$ ... External clock input (Slave))

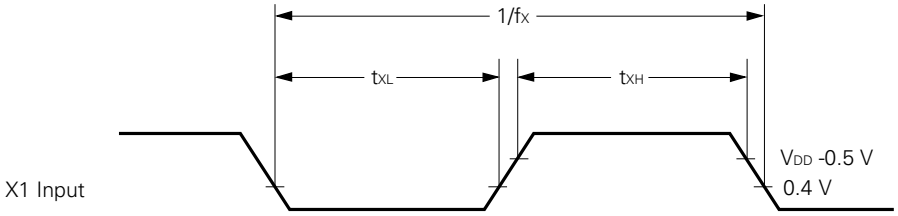
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high and low level widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low level widths	t_{SBL}			t_{KCY4}			ns
SB0, 1 high level widths	t_{SBH}			t_{KCY4}			ns

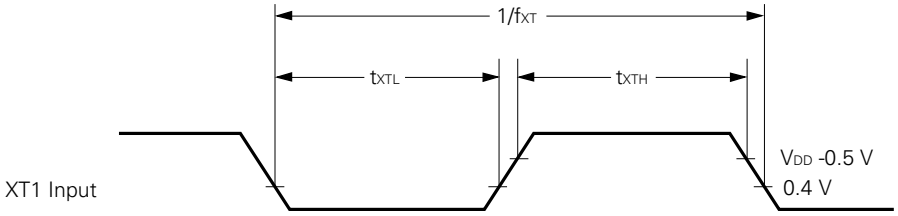
***** R_L and C_L denote load resistor and load capacitance of SO output lines.

AC Timing Test Points (Except X1 and XT1 Inputs)

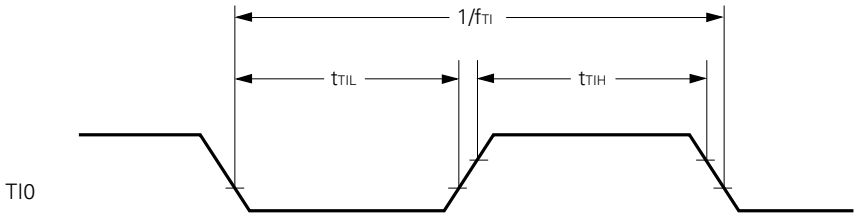


Clock Timings



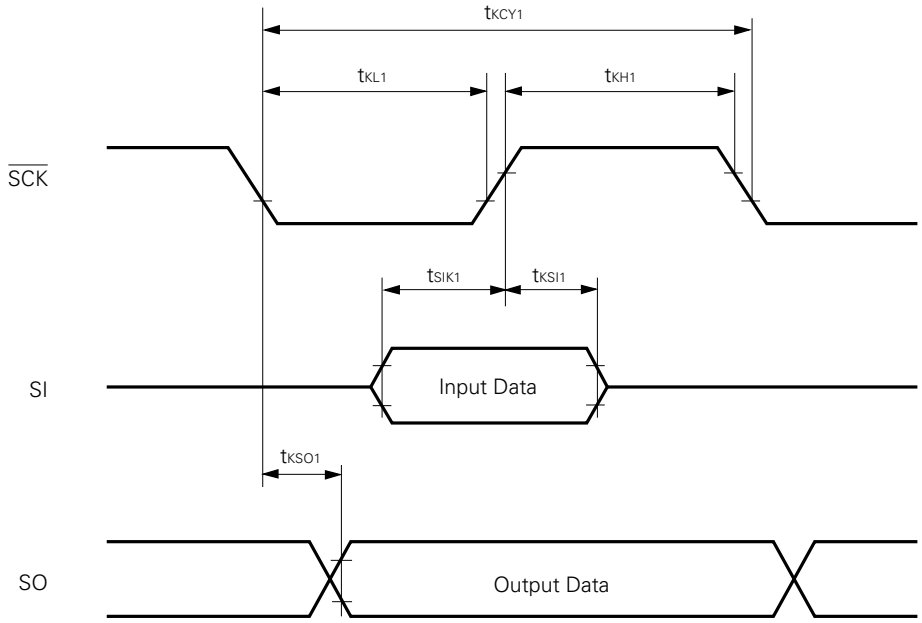


TI0 Timing

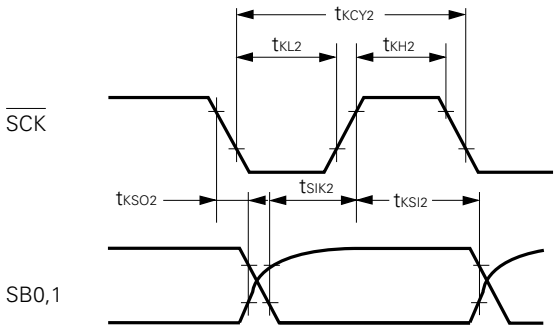


Serial Transfer Timing

3-wired serial I/O mode:

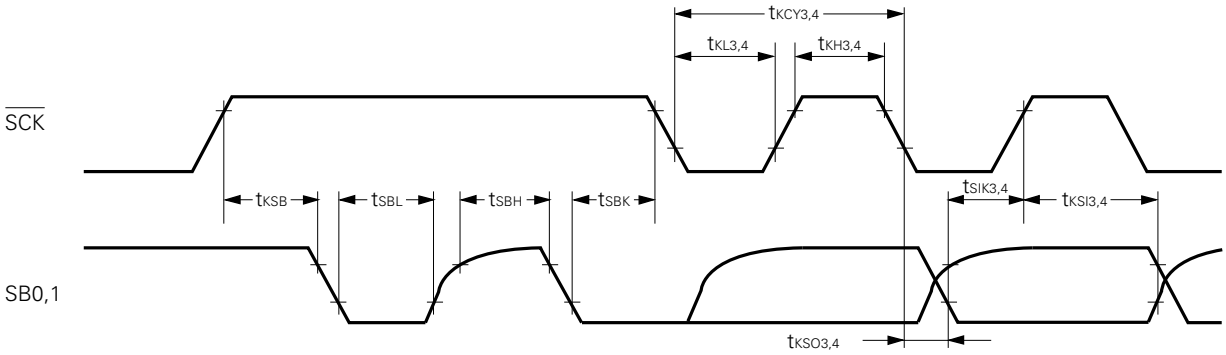


2-wired serial I/O mode:

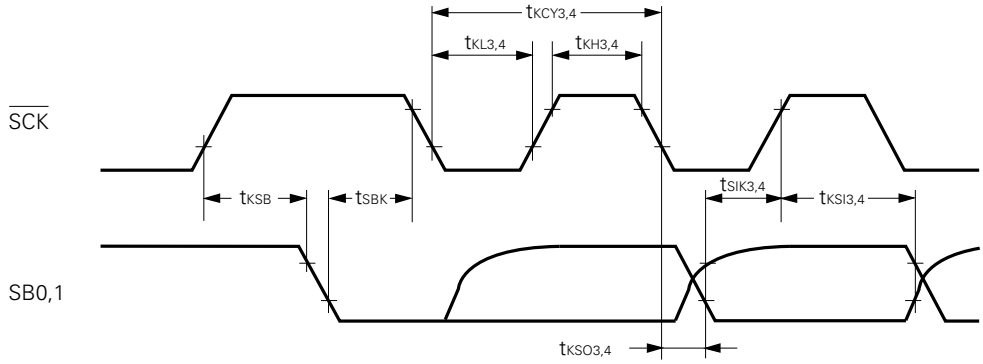


Serial Transfer Timing

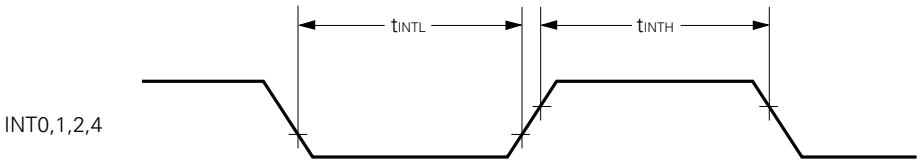
Bus release signal transfer:



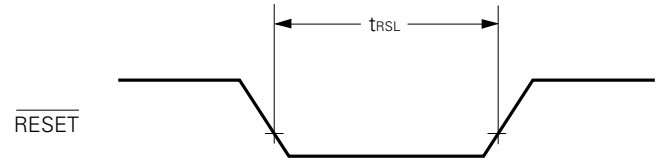
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.0		6.0	V
Data retention power supply current***1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time***2**	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt request		***3**		ms

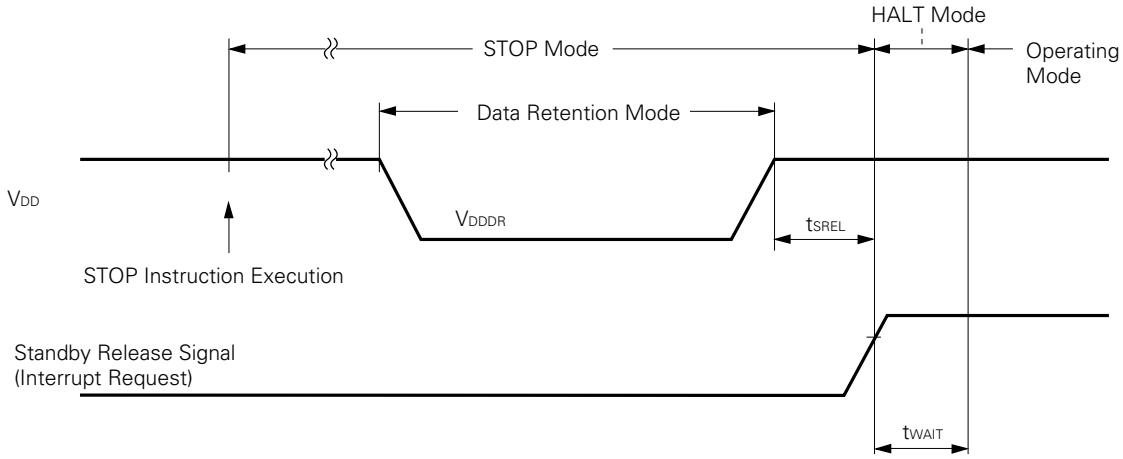
* **1.** Current to the on-chip pull-up resistor and power-on reset circuit (mask option) is not included.

2. Oscillation stability wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.

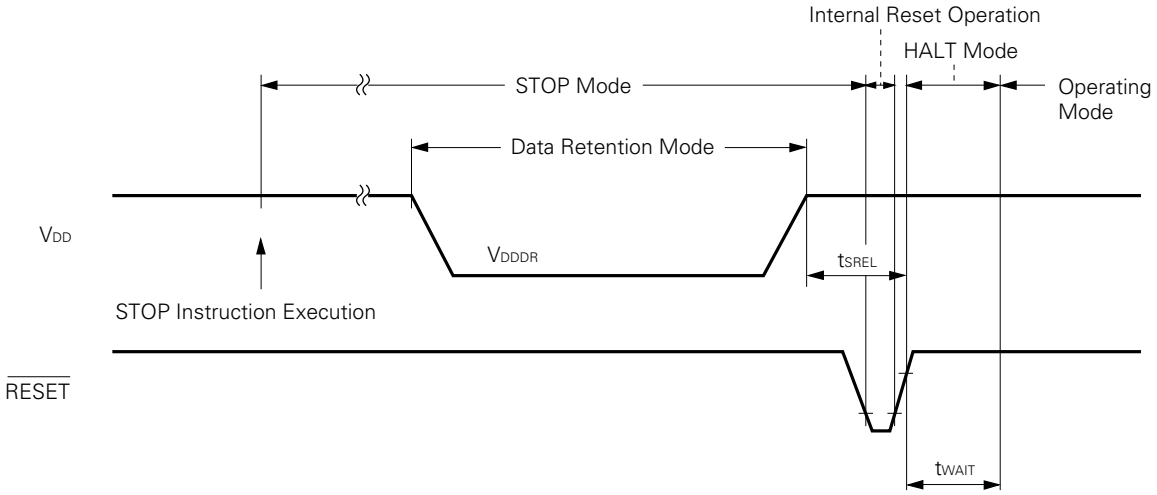
3. According to the setting of the basic interval timer mode register (BTM). (see below)

BTM3	BTM2	BTM1	BTM0	Wait Time	
				Values at fx = 6.0 MHz in Parentheses	Values at fx = 4.19 MHz in Parentheses
—	0	0	0	2^{20}/fx (approx. 175 ms)	2^{20}/fx (approx. 250 ms)
—	0	1	1	2^{17}/fx (approx. 21.8 ms)	2^{17}/fx (approx. 31.3 ms)
—	1	0	1	2^{15}/fx (approx. 5.46 ms)	2^{15}/fx (approx. 7.82 ms)
—	1	1	1	2^{13}/fx (approx. 1.37 ms)	2^{13}/fx (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



DC PROGRAMMING CHARACTERISTICS (Ta = 25 ±5 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except X1 and X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1 and X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Output voltage low	V_{OL}	I_{OH} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MDI = V_{IH}			30	mA

Note 1. V_{PP}, including overshoot, should not exceed +13.5 V.
2. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (Ta = 25 ±5 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V) (1/2)

PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time*2 (to MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time*2 (from MD0 ↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0 ↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD0 ↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse widths	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse widths	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1 ↑)	t_{MOS}	t_{CES}		2			μs
Data output delay time from MD0 ↓	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs

* **1.** The corresponding μPD27C256 symbol.
2. Internal address signal is incremented by one on the rise of fourth X1 input and is not connected to the pin.

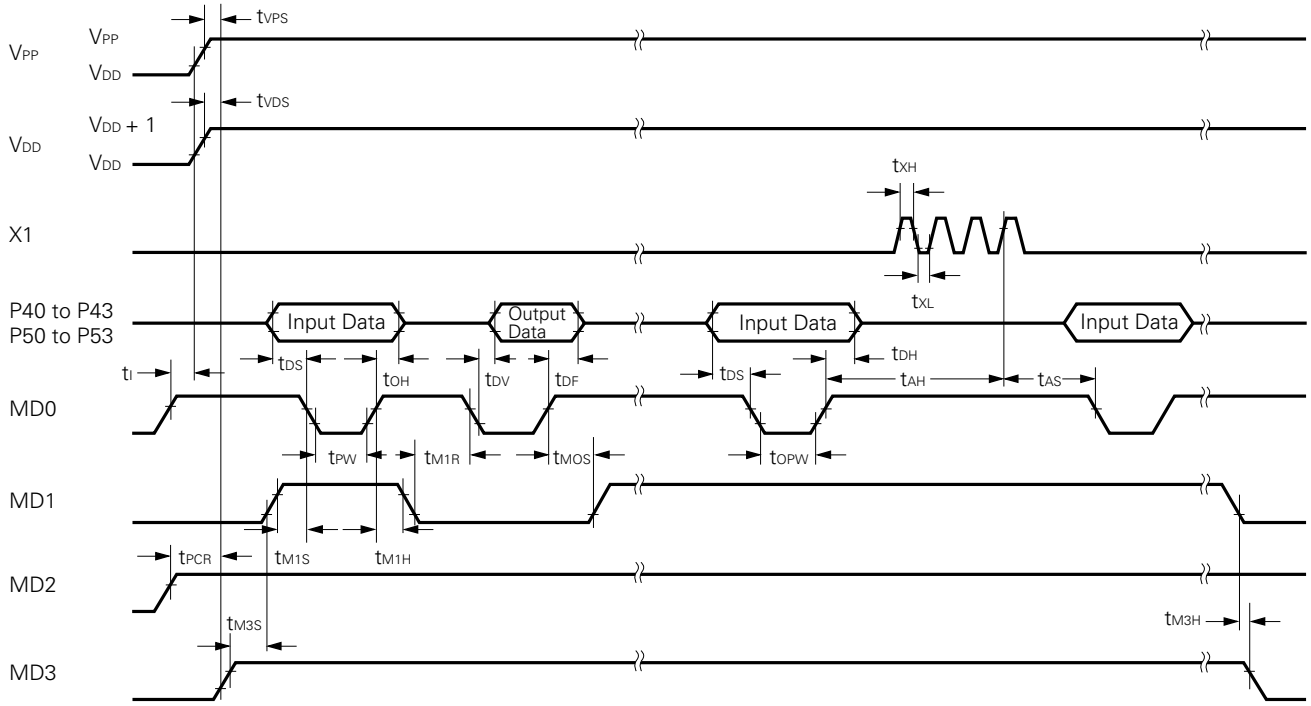
AC PROGRAMMING CHARACTERISTICS (T_a = 25 ±5 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V) (2/2)

PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
MD1 hold time (from MD0 ↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50\ \mu s$	2			μs
MD1 recovered time (to MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	——		10			μs
X1 input high and low level widths	t_{XH}, t_{XL}	——		0.125			μs
X1 input frequency	f_X	——				4.19	MHz
Initial mode set time	t_I	——		2			μs
MD3 setup time (to MD1 ↑)	t_{M3S}	——		2			μs
MD3 hold time (from MD1 ↓)	t_{M3H}	——		2			μs
MD3 setup time (to MD0 ↓)	t_{M3SR}	——	When reading program memory	2			μs
Data output delay time from address*2	t_{DAD}	t_{ACC}	When reading program memory	2			μs
Data output hold time from address*2	t_{HAD}	t_{OH}	When reading program memory	0		130	ns
MD3 hold time (from MD0↑)	t_{M3HR}	——	When reading program memory	2			μs
Data output float delay time from MD3↓	t_{DFR}	——	When reading program memory	2			μs

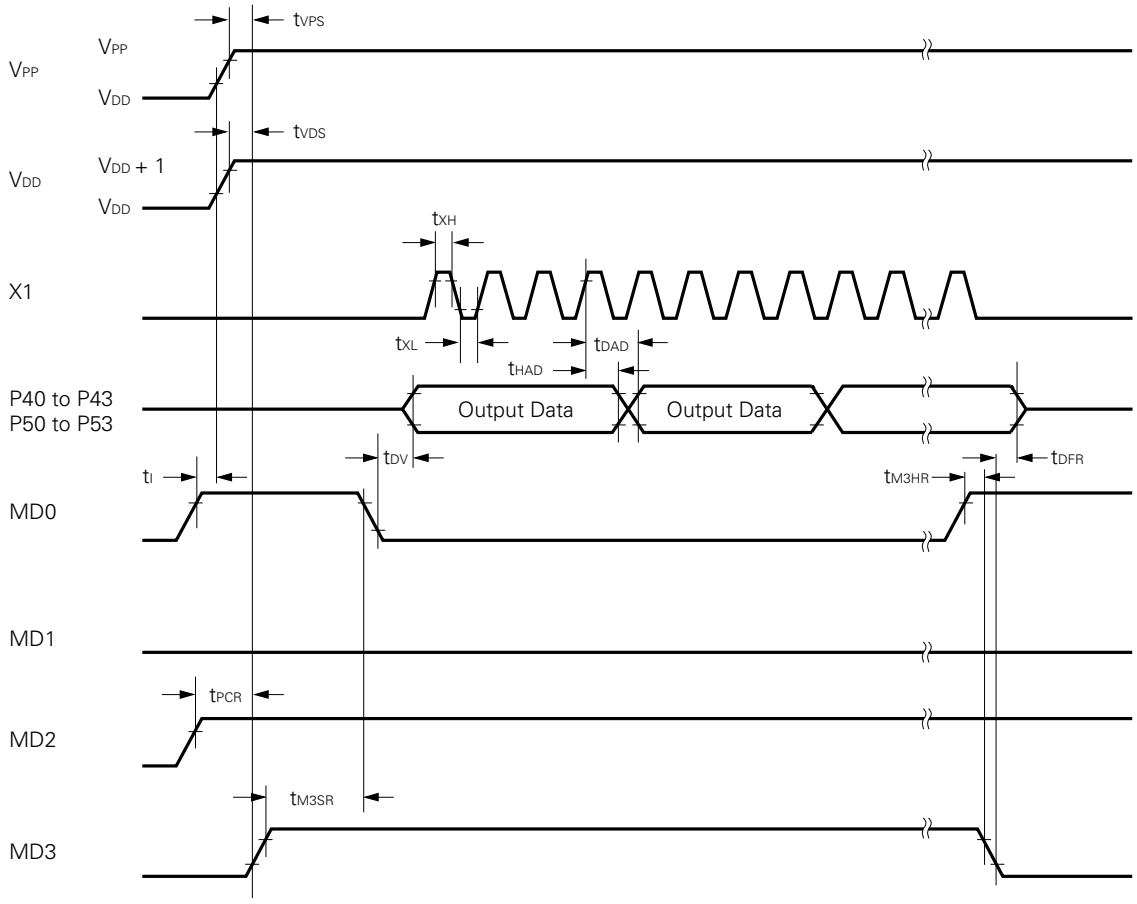
* **1.** The corresponding μPD27C256 symbol.

2. Internal address signal is incremented by one on the rise of fourth X1 input and is not connected to the pin.

Write Timing of Program Memory

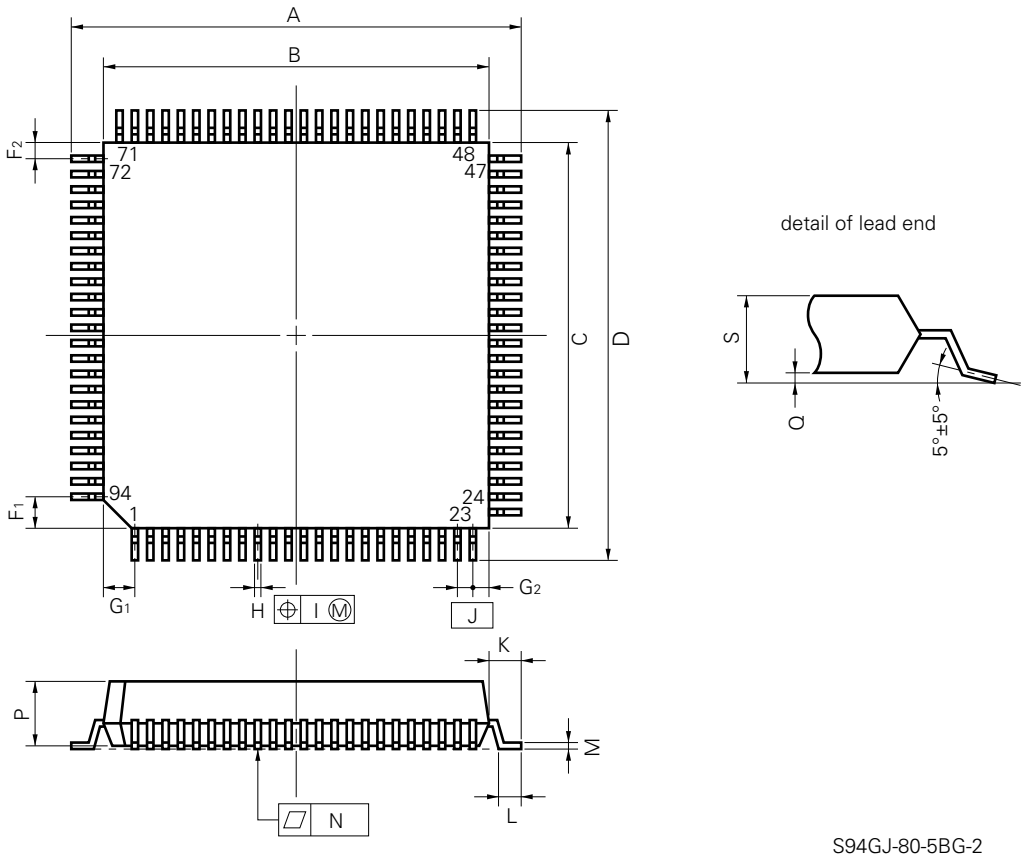


Read Timing of Program Memory



7. PACKAGE INFORMATION

94 PIN PLASTIC QFP (□20)



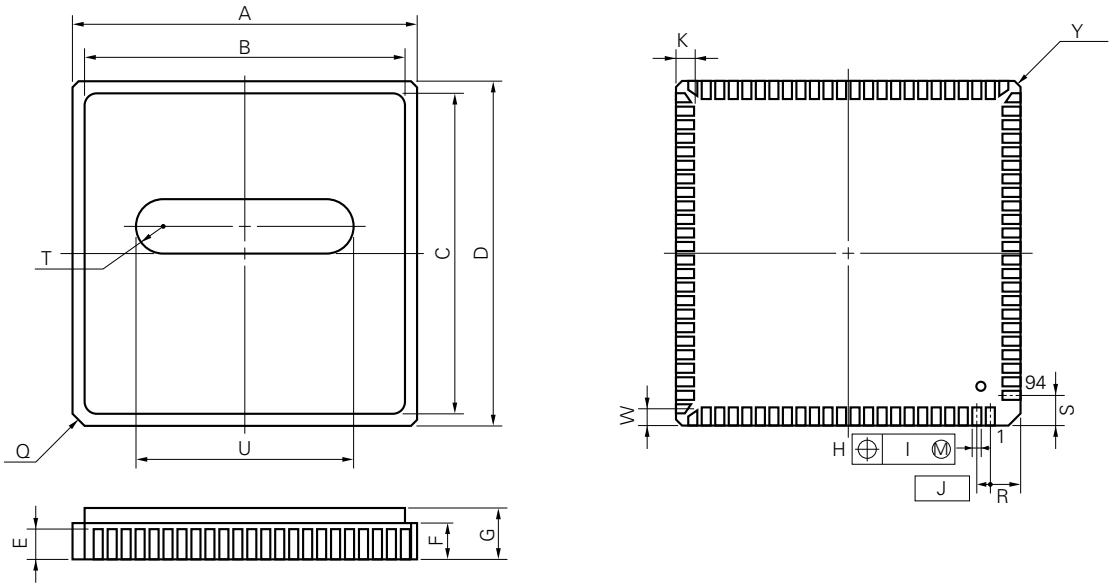
S94GJ-80-5BG-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	1.6	0.063
F_2	0.8	0.031
G_1	1.6	0.063
G_2	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.158 MAX.

94 PIN CERAMIC WQFN



X94KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	18.0	0.709
C	18.0	0.709
D	20.0±0.4	$0.787^{+0.017}_{-0.016}$
E	1.94	0.076
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 1.0	C 0.039
R	1.6	0.063
S	1.6	0.063
T	R 1.75	0.069
U	11.5	0.453
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$

8. RECOMMENDED SOLDERING CONDITIONS ★

This product should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the **information document "Surface Mount Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 8-1 Surface Mount Type Soldering Conditions

μPD75P238GJ-×××-5BG : 94-pin plastic QFP (□20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above); Number of times: Once, Time limit: 7 days* (125 °C prebaking requires 10 hours thereafter)	IR30-107-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above); Number of times: Once, Time limit: 7 days* (125 °C prebaking requires 10 hours thereafter)	VP15-107-1
Pin part heating	Pin part temperature: 300 °C max.; Duration: 3 sec. max., (per device side)	———

* For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65% RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

APPENDIX A. DEVELOPMENT TOOLS

The following support tools are available for system development using the μPD75P238.

Hardware	IE-75000-R***1** IE-75001-R	75X series in-circuit emulator
	IE-75000-R-EM***2**	IE-75000-R/IE-75001-R emulation board
	EP-75238GJ-R EV-9200G-94	μPD75P238 emulation probe 94-pin conversion socket EV-9200G-94 is provided
	PG-1500	PROM programmer
	PA-75P238GJ	PG-1500 connected with μPD75P238GJ PROM program adapter
	PA-75P238KF	PG-1500 connected with μPD75P238KF PROM program adapter
Softwar	IE control program	Host machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A***3**) IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

***** **1.** Maintenance product
2. Not incorporated in IE-75001-R
3. The task swap function, which is provided with Ver.5.00/5.00A. is not available with this software.

Remarks For development tools manufactured by a third party, see the **"75X Series Selection Guide" (IF-151)**.

APPENDIX B. RELATED DOCUMENTS ★

Device Related Documents

Document Name	Document No.
User's Manual	
Instruction Application Table	
75X Series Selection Guide	

Development Tools Related Documents

Document Name			Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		
	IE-75000-R-EM User's Manual		
	EP-75238GJ-R User's Manual		
	PG-1500 User's Manual		
Software	RA75X Assembler Package User's Manual	Operation Volume	
		Language Volume	
	PG-1500 Controller User's Manual		

Other Documents

Document Name	Document No.
Package Manual	
Surface Mount Technology Manual	
Quality Grade on NEC Semiconductor Devices	
NEC Semiconductor Device Reliability & Quality Control	
Electrostatic Discharge (ESD) Test	
Semiconductor Devices Quality Guarantee Guide	
Microcomputer Related Products Guide Other Manufactures Volume	

Note The contents of the above related documents are subjected to change without notice. The latest documents should be used for design, etc.

[MEMO]

M4 92.6